IN THE CLAIMS

Amend claims as follows:

[1 (c1)] (Currently Amended) Apparatus for performing parallel tests (of logic and memory) for semiconductor devices having logic and memory macro with BIST circuits, comprising:

voltage isolation elements for logic and memory circuits having individual separate isolated independent clocking paths to each logic and memory macro circuits;

a clocking system including clocking isolation elements for logic and memory circuits;

scan chain ~~by-pass~~bypass isolation elements;

to enable and disable the BIST ~~whereby the testing of~~which tests the memory macro circuits ~~is performed~~ while the logic scan chain results are read out.

[2 (c2)] (Original) The apparatus of claim 1 wherein the bypass isolation elements are initiated by a control signal.

[3 (c3)] (Original) The apparatus of claim 2 wherein the control signal is provided by a primary input from control circuit.

[4 (c4)] (Original) The apparatus of claim 2 wherein the control signal is provided by a latch.

[5 (c5)] (Original) The apparatus of claim 2 wherein the control signal is applied to a latch.

[6 (c6)] (Original) The apparatus of claim 5 wherein the latch provides the control signal to a multiplexer in each memory macro.

[7 (c7)] (Original) The apparatus of claim 6 wherein the control signal places the apparatus into bypass mode by selecting a scan in signal which loads logic test patterns into the BIST circuits.

[8 (c8)] (Original) The apparatus of claim 7 wherein after the BIST is completed the apparatus is taken out of bypass mode and the results are unloaded.

[9 (c9)] (Original) The apparatus of claim 6 wherein the clocking system includes a memory test lock which allows a logic test pattern to be loaded and unloaded independent of the memory clock.

[10 (c10)] (Original) The apparatus of claim 9 wherein a signal to the clocking system is applied by an external tester to a clock multiplier and control circuit.

[11 (c11)] (Original) The apparatus of claim 9 wherein a signal to the clocking system is applied by an external tester to a clock generator located on the semiconductor device.

[12 (c12)] (Original) A method for performing parallel tests of logic and memory on a semiconductor device having logic with BIST and memory circuits comprising:

separating the logic and memory circuits using isolation elements;

clocking the logic and memory circuits;

enabling and disabling the BIST scan chain bypass isolation elements; and

testing the memory circuits while the logic scan chain results are read out.

[13 (c13)] (Original) The method of claim 12 including testing the bypass isolation elements by a control bypass signal.

[14 (c14)] (Original) A method for performing parallel tests of logic and memory macro on a semiconductor device having logic with BIST and memory circuits comprising:

verifying scan chain and BIST operation;

loading BIST patterns using global clocking;

placing the device into a bypass mode wherein the memory macro circuits are isolated from the scan chains;

generating separate test clock signals to both memory macro circuits and logic circuits; and

running the scan chains in parallel with BIST.